REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action, claims 1-16, 21-27 and 33-39 were pending and rejected. In this response, claims 33-39 have been canceled without prejudice. Claims 1-13 and 21-22 have been amended. The support can be found in page 2 of the Specification, for example. No new matter has been added.

Claims 1, 3, 10, 12, 21, 33-35, and 37-38 were objected because alleged new matters and claims 1, 3, 10-12, 21, and 33-39 were rejected under 35 U.S.C. 112 first paragraph and claims 1, 3-12, and 21-27 were rejected under 35 U.S.C. 112, second paragraph.

In view of the foregoing amendments, some of the objections and 35 U.S.C. 112 rejections have been overcome. It is respectfully submitted that the rest of the limitations of claims are fully supported by the specification. For example, Figures 1-2 clear disclose the dedicated interrupt vector address spaces for different processors. Withdrawal of the rejection is respectfully requested.

Claims 1-3 and 21-23 are rejected under U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,006,247 of Browning ("Browning") in view of U.S. Patent No. 6,167,479 of Hartnett et al. ("Hartnett") and U.S. Patent No. 6,611,911 of O'Shea ("O'Shea"), and U.S. Patent No. 6,615,303 of Endo et al. ("Endo"), a combination of four (4) different references.

It is respectfully submitted that claims 1-16 and 21-27 as amended include limitations that are not disclosed or suggested by the cited references, individually or in combination. Specifically, for example, independent claim 1 recites as follows:

> 1. A method for handling exceptions in a multi-processor system, the method comprising:
> receiving an exception within a processor which is one of a plurality of processors of the multi-processor system which is implemented within a control card of a network element for routing data in networks, wherein each of the plurality of processors in the multi-processor system shares a memory within the multi-processor system, wherein the memory includes a common interrupt handling vector address space shared by the plurality of the processors and a dedicated interrupt handling vector address space for each of the plurality of the processors; and
> executing one or more instructions at an address associated with a type of the received exception within the common interrupt handling vector address space of the memory, wherein the one or more instructions cause the processor to modify based on an identification of the processor an execution flow of the received exception to execute an interrupt handler located within a respective dedicated interrupt handling vector address spaces associated with the processor,
> wherein the plurality of processors includes a first processor and a second processor, the first processor executing a first operating system and the second processor executing a second operating system, the second operating system being different from the first operating system, and
> wherein the first processor along with the first operating system is configured to handle routing of data received within the network element and the second processor along with the second operating system is configured to handle provisioning and configuration of the network element.

(Emphasis added)

Independent claim 1 as amended includes limitations of a common interrupt handling vector address space shared by multiple processors running multiple different operating systems, where one of the processors is configured to handle routing data within a network element and another one of the processors is configured to handle provisioning and configuration of the network element. It is respectfully submitted that the above limitations are absent from the cited references, individually or in combination.

Although Browning discloses handing exceptions of multi-thread of a multi-processor system, there is no disclosure or suggestion within Browning that each of the processors is running different operating systems. While Endo discloses running multiple operating systems, such multiple operating systems appear run at a single processor.

In addition, none of Browning and/or Endo discloses such techniques can be implemented within a control card of a network element for routing data for networks. Further, there is no disclosure or suggestion within Browning and/or Endo of a first processor having a first operating system is configured to handle routing data within the network element, while a second processor having a second operating system is configured to handle provisioning and configuration of the network element. It is respectfully submitted that Hartnett and O'Shea also fail to disclose or suggest the limitations set forth above.

Furthermore, there is no suggestion within the cited references to combine with each other. As described above, for example, Browning is related multi-threads of multi-processors while Endo is related multi-operating systems of a sole processor. Given the significantly different architectures, one with ordinary skill in the art, based on the teachings of Browning and Endo, as well as Hartnett and O'Shea (e.g., four different references), would not combine these four references because such a combination lacks reasonable expectation of success. Therefore, independent claim 1 is patentable over Browning in view of Endo, Hartnett, and O'Shea.

Similarly, independent claims 12 and 21 include limitations similar to those set forth above with respect to claim 1. Thus, for the reasons similar to those discussed above, it is respectfully submitted that claims 12 and 21 are patentable over the cited references.

Given that the rest of the claims depend from one of the above independent claims, it is respectfully submitted that the rest of the claims are also patentable over the cited references.

Claims 4-5 and 24-25 were rejected under U.S.C. 103(a) as being unpatentable over Browning in view of Endo, Hartnett, O'Shea, U.S. Patent No. 6,314,500 of Rose ("Rose"), and U.S. Patent No. 6,745,336 of Martonosi et al. ("Martonosi"), a combination of six (6) different references.

Claims 6-7 and 26-27 were rejected under U.S.C. 103(a) as being unpatentable over Browning in view of Endo, Hartnett, O'Shea, Rose, Martonosi, U.S. Patent No. 5,113,523 of Colley ("Colley"), and U.S. Patent No. 6,539,440 of Stracovsky ("Stracovsky") a combination of eight (8) different references.

Claims 8-16 were rejected under U.S.C. 103(a) as being unpatentable over Browning in view of Endo, Hartnett, O'Shea, Rose, Martonosi, Colley, and U.S. Patent No. 5,805,790 of Nota ("Nota") a combination of eight (8) different references.

It is respectfully submitted that the cited references (e.g., 6-8 different references) also fail to disclose or suggest the limitations set forth above. There is no suggestion within these 6-8 different references to combine with each other. The fact that some of these references merely mentioned certain terms of the limitations set forth above would not enable one with ordinary skill in the art to combine these references because such a combination lacks motives and/or reasonable expectation of success. Such a combination can only be based on the impermissible hindsight of Applicant's own disclosure. Therefore, claims 1-16 and 21-27 as amended are patentable over the cited references. Withdrawal of the rejections is respectfully requested.

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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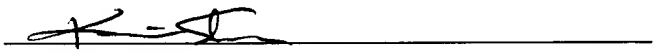

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